

Electrical Characterization of InGaZnO-Based Thin Film Transistor Fabricated by Three-Mask Process

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ORIGINAL RESEARCH

Abstract- Indium Gallium Zinc Oxide (InGaZnO) stands as a viable alternative material to amorphous silicon to produce thin-film transistors owing to its remarkable electrical and optoelectronic properties, robust chemical stability, and the prospect of low-temperature processing. Nevertheless, efforts are being made to optimize the design with improved performance at minimal processing steps and reduced costs. In this study, a Top Contact Top Gate configuration is used for InGaZnO thin-film transistor fabrication via a three-step lithography process, subsequently measuring device current-voltage characteristics and extracting key parameters. For the best device, a threshold voltage of -9 V , $\frac{ON}{OFF}$ ratio in the range of 10^3 , maximum mobility of $1.15\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, sub-threshold slope in the range of 10^3 mV/decade , and maximum interface trap density of $1.53 \times 10^{14}\text{ cm}^{-2}\text{eV}^{-1}$ were determined at maximum applied voltage of 5 V . All these parameters depend on the applied voltage.

Keywords- Electron Mobility, Indium Gallium Zinc Oxide (InGaZnO), Lithography, Parameter Extraction, Thin Film Transistor

1 INTRODUCTION

Thin-film transistors (TFTs) are distinct metal-oxide-semiconductor field-effect transistors (MOSFETs) created through the deposition of a stacked thin layers consisting of an active semiconductor (mesa), gate oxide, and metal contacts onto an insulating substrate (Pandey et al., 2021). Unlike traditional silicon-based MOSFETs, which usually require the deposition of active silicon material at high temperatures (typically greater than 1000°C), TFTs require low-temperature processing (typically less than 650°C) (Petti et al., 2016). As a result, TFTs, as fundamental electronic devices, have attracted increasing attention due to their wide range of applications, including displays (such as flat panel, organic light-emitting diodes, and liquid crystal displays), circuits (flexible, printable, and transparent circuits), sensors (including temperature, chemical, and optical sensors), and other areas like light-emitting applications (Cao & Liang, 2020). Several active channel materials have been used in the development of thin-film transistors, such as polycrystalline silicon (Brotherton, 1995), amorphous silicon (Han et al., 2022), Zinc Oxide (Jiang et al., 2017), Indium Gallium Zinc Oxide (Zhu et al., 2021), organic semiconductors (Reese et al., 2004), and carbon nanotubes (Lu & Franklin, 2020). Currently, most flat-panel displays are based on amorphous silicon TFT because of their simple fabrication and low cost (Cao & Liang, 2020).

Nevertheless, a major constraint of amorphous silicon TFT technology is its low electron mobility, which limits its use in next-generation displays that require high transparency, fast response speed, and large-area processing. Amorphous indium gallium zinc oxide (InGaZnO) is an emerging replacement material for next generation displays owing to its excellent electrical characteristics, high transparency, easy synthesis, and good chemical stability (Ahn & Cho, 2017), (Huo et al., 2021). Although considerable research has been conducted on amorphous InGaZnO TFTs on flexible substrates and transparent displays to achieve an electron mobility of $30\text{ cm}^2/\text{s}$, there remains a need for an optimal design to realize the desired display resolution and pixel circuits. Efforts have been made towards this goal in previous studies using a variety of heat-treatment methods, solution-grown InGaZnO active media, and interface engineering (Zhao et al., 2020), high-k gate oxides such as hafnium oxide (Samanta et al., 2020), and multiple active-layer structures.

Ahn and Cho (2017) reported the use of double-layered oxide TFTs by burying an indium tin oxide (ITO) conducting layer below the InGaZnO oxide layer to improve electrical performance. The interface between the metal contacts and active semiconductor layer was found to play a critical role in device performance; thus, to regulate the interfaces between the metal contacts and the InGaZnO channel, an interface engineering method of bifunctional acid modification was used (Zhao et al., 2020). Furthermore, with respect to the device fabrication process, the structure most frequently used in modern display technology is the bottom-gate and top-contact (TCBG)-type device. Nonetheless, the TCBG device suffers from several drawbacks due to the exposure of the channel surface to the atmosphere, resulting in instability as a result of gas diffusion alongside adsorption, and outgassing (desorption) from the surface. Enhancing stability can be achieved by adopting a top-gate with top-

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Section B- ELECTRICAL/COMPUTER ENGINEERING & RELATED SCIENCES

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contact (TCTG) configuration (Ahn & Cho, 2017). In addition, the atomic layer deposition (ALD) technique has been previously employed for depositing gate oxides in InGaZnO-based thin-film transistors (Samanta et. al., 2020) (Woo et. al., 2012) and in other devices such as metal-insulator-metal diodes fabrication (Etor et. al., 2022) because of its unique advantage of conformal deposition on diverse structures using sequential and self-limiting chemical reactions. Therefore, ALD technique is adopted for the deposition of the gate oxide in this work. Most of the literature examined demands intricate fabrication processes, often entailing more than three mask-processing steps.

To this end, we propose a top-contact top-gate (TCTG) configuration InGaZnO-based TFT using three photolithography (mask) steps. In addition, we introduce a unique method for etching molybdenum contacts in thin-film transistor fabrication using wet chemical etching employing hydrogen peroxide. The electrical current-voltage characteristics of the fabricated TFT were measured and used to extract the key device parameters.

2 METHODOLOGY

2.1 FABRICATION PROCESS

The initial substrate utilized was a 6-inch p-type Si wafer (150 mm), sourced from MIT.Nano. Following the conventional wafer-cleaning procedure, approximately 420 nm thick silicon oxide (SiO_2) film was grown on the Si wafer by plasma-assisted chemical vapor deposition (PECVD). This SiO_2 layer served as the insulating surface on which the TFT would be fabricated. The active material, InGaZnO (IGZO), was then deposited onto the insulating substrate by DC sputtering, maintaining a pressure of 1 milli Torr, a power of 100 Watts, and a gas mixture of argon (Ar) and oxygen (O_2) in the ratio 20 to 1 respectively. Next, the IGZO mesa was fabricated using photolithography and etching. In this process, IGZO was first spin-coated with a photoresist (AZ3312 using PicoTrack, a wafer track that automatically coats a photoresist), followed by direct laser writing of the pattern with a maskless aligner (MLA) before development using tetramethylammonium hydroxide (TMAH) to obtain the mask shown in Figure 2(a). Subsequently, the IGZO was etched using a wet chemical mixture of HCl and H_2O in a ratio of 1:9 for approximately 40 s. This is followed by stripping of the photoresist mask, using the standard procedure of sequential cleaning with acetone, isopropanol, and oxygen plasma, to obtain the IGZO mesa structure shown in Figure 2(b). Furthermore, the aluminum oxide (Al_2O_3) gate oxide was deposited via atomic layer deposition onto the IGZO mesa.

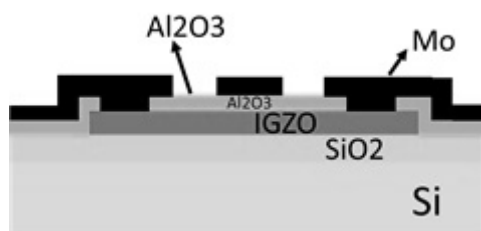


Fig. 1: Structure of the Thin Film Transistor

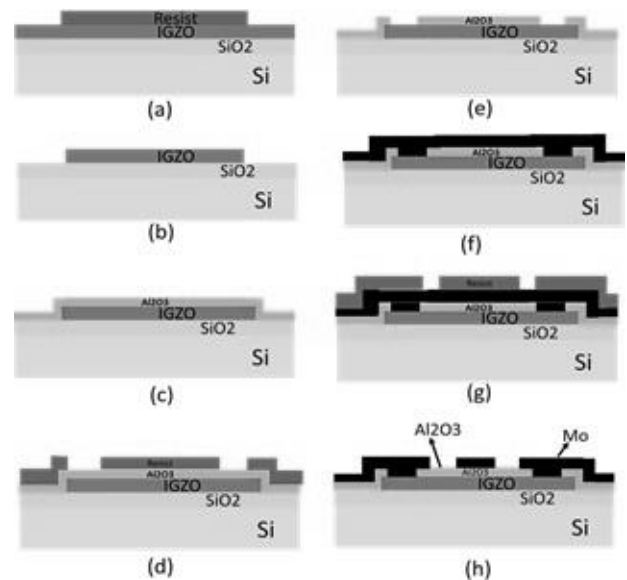


Fig. 2: InGaZnO TFT device fabrication process. (a) 1st mask process to define the InGaZnO mesa, (b) InGaZnO wet etching followed by photoresist stripping to obtain the mesa layer, (c) Al_2O_3 gate oxide deposition by ALD, (d) 2nd mask process to define the source and drain region (e) by exposing oxide - Al_2O_3 via wet etching followed by photoresist stripping, (f) Mo deposition by sputtering, (g) 3rd mask process to define the gate region and isolate the source from the drain (h) via opening in Mo for source, drain and gate isolation - Mo wet etching followed by photoresist stripping.

Approximately 20 nm (200 cycles) of ALD Al_2O_3 was deposited at 250°C, employing the standard trimethylaluminum (TMA) and H_2O processes. Afterward, the source and drain regions were defined by photolithography to obtain the second mask (Figure 2(d)), followed by the opening of the oxide to expose the IGZO source and drain region. Using the photoresist mask shown in Figure 2 (d) as an etch stop, Al_2O_3 was etched using HF for 1–2 min before rinsing in H_2O , then followed by stripping of the photoresist mask to obtain the structure shown in Figure 2 (e).

Finally, approximately 30 nm molybdenum (Mo) film was grown on the entire surface by direct current sputtering under a pressure of 2 milli Torr, power of 100 W, and in argon atmosphere. In this process, Mo was deposited as a contact for the source, drain, and gate regions, as shown in Figure 2 (f). A third mask (Figure 2 (g)) was created using photolithography to define the regions of the source, drain, and gate contacts to prevent short circuits. This mask was used as an etch stop to define the via in Mo by wet etching ($\text{H}_2\text{O}_2:\text{H}_2\text{O} = 1:1$) to isolate the source, drain, and gate contacts after Mo etching and resist stripping, thereby obtaining the complete structure shown in Figure 2 (h).

2.2 ELECTRICAL CHARACTERIZATION

Electrical characterization of the fabricated IGZO TFT was carried out on a probe station using a B1500A Semiconductor Device Analyzer. The TFTs current-voltage characteristics were measured, while the threshold voltage V_t and conductance parameter K were extracted for different gate lengths (L) and widths (W). The output I-V characteristics were acquired by sweeping

the drain voltage and measuring the resulting drain current, all while maintaining a constant gate voltage. Similarly, the transfer I-V characteristics were acquired by varying the gate voltage and measuring the corresponding drain current, all while maintaining a constant drain voltage.

2.3 PARAMETER EXTRACTION

To extract the device parameters, the transistor drain current equation in the saturation region is considered as follows:

$$i_D = \frac{K}{2}(v_{GS} - V_t)^2 = \frac{K}{2}(v_{Dsat})^2 \quad (1)$$

The parameter v_{GS} is the gate to source voltage, while v_{Dsat} is the drain-source voltage at saturation. The parameter V_t is the threshold voltage defined as the minimum gate voltage required to turn "ON" the transistor. The parameter K is called the conduction parameter, defined as:

$$K = \frac{W}{L} \mu_n C_{ox} \quad (2)$$

where μ_n , W , L , and C_{ox} are the electron mobility, channel width, channel length, and oxide capacitance per unit area, respectively. In this case, C_{ox} is determined from $C_{ox} = \frac{\epsilon}{tox}$ where ϵ is the permittivity of the insulating medium and tox is the thickness of the insulating oxide. The dielectric constant of aluminum oxide was taken to be 8.5. The electron mobility, μ_n , can be obtained using Eq. (3) (Huo et. al., 2021), (Neamen, 2007):

$$\mu_n = \frac{L}{W} \frac{g_m}{C_{ox} v_{Dsat}} \quad (3)$$

where

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_D = constant} \quad (4)$$

or

$$g_m = K(v_{GS} - V_t) = K v_{Dsat} = \frac{W}{L} \mu_n C_{ox} v_{Dsat} \quad (5)$$

The transconductance g_m was determined from the measured data by using the gradient function in MATLAB to calculate the derivative of the transfer characteristics. The ON-OFF current ratio is another crucial parameter, which is defined as:

$$ON - OFF = \frac{i_{D-ON}}{i_{D-off}} \quad (6)$$

where i_{D-ON} is the maximum drain current while i_{D-off} is the minimum drain current.

The quantity S is the sub-threshold swing defined as:

$$S = \left(\frac{\partial \log i_D}{\partial v_{GS}} \right)^{-1} \quad (7)$$

The sub-threshold region indicates a decrease in the drain current with gate bias. Achieving a lower value of S is advantageous, especially in low-voltage, low-power scenarios, such as when employing MOSFETs as switches in digital logic and memory applications (Sze et. al., 2021). The sub-threshold swing was determined from the measured I-V transfer characteristics while the current axis (y-axis) was plotted on a logarithmic scale.

The interface trap density can be obtained from the sub-threshold region using the equation below (Ahn & Cho, 2017; Lyu & Lee, 1993):

$$D_{it} = \frac{C_{ox}}{q} \left(\frac{S(\log e)}{k_B T/q} - 1 \right) \quad (8)$$

where the parameter k_B is the Boltzmann constant, q is the electronic charge, C_{ox} is the gate oxide capacitance per unit area, and T is the absolute temperature.

The threshold voltage V_t can be determined from the transfer I-V characteristics i_D vs v_{GS} , using linear extrapolation in the linear region (Dobrescu et. al., 2000). Thus, the derivative of the drain current with respect to gate to source voltage $\frac{\Delta i_D}{\Delta v_g}$ was plotted from the measured data using the gradient function in MATLAB while an inflection point was obtained at a particular gate voltage. A tangent was drawn on the transfer characteristics (i_D vs v_{GS}) at the gate voltage corresponding to the maximum $\frac{\Delta i_D}{\Delta v_g}$ (inflection point) while the threshold voltage was obtained by extrapolating this tangent to the voltage axis.

3 RESULTS AND DISCUSSION

As shown in Figure 3, the optical image of the fabricated device, the IGZO mesa was entirely covered by a Mo contact layer, thereby protecting the mesa from environmental degradation. The source, drain, and gate were extended to the Mo-measurement contact region.

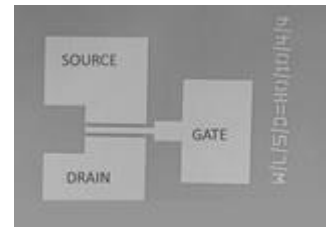


Fig. 3: Image of the fabricated IGZO TFT obtained from an optical microscope.

The output characteristics of the fabricated device for a width/length = 30 μ m/2 μ m is shown in Figure 4. The drain voltage was varied from 0 to 5 V, with a constant gate voltage set at 0 V, decreasing down to -16 V. It is evident from the I-V characteristics shown in Figure 4 that the transistor functions in "depletion mode." This means it did not switch "OFF" when the gate voltage was at 0 V (indicated by the blue line), and instead, a negative gate voltage is needed to turn the transistor "OFF", resulting in a transistor threshold voltage obtained at a negative gate voltage (Neamen, 2007). For the same device, the transfer characteristics was acquired by sweeping the gate voltage and measuring the corresponding drain current at a constant drain voltage of 2 V, as illustrated in Figure 5. Thereafter, the threshold voltage was determined by the linear extrapolation of i_D vs v_{GS} at the maximum $\frac{\Delta i_D}{\Delta v_g}$. A

tangent (black broken line in Figure 5) was drawn at the gate voltage associated with the maximum of $\frac{\Delta I_d}{\Delta V_g}$, while the threshold voltage was extrapolated to be approximately -9 V (Figure 5) for the fabricated transistor with design parameters $W/L = 30\mu\text{m}/2\mu\text{m}$, 8 nm IGZO and 30 nm Al_2O_3 .

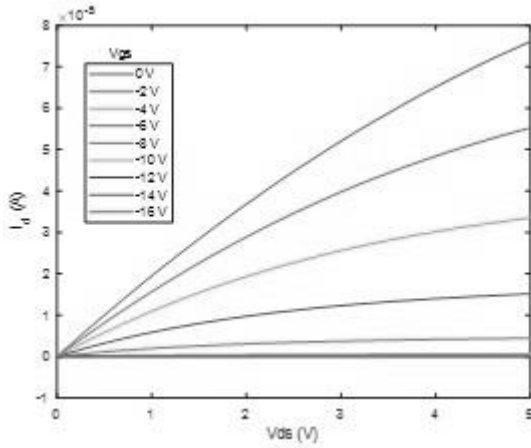


Fig. 4: Output characteristics of the IGZO TFT device fabricated for $W/L = 30\mu\text{m}/2\mu\text{m}$.

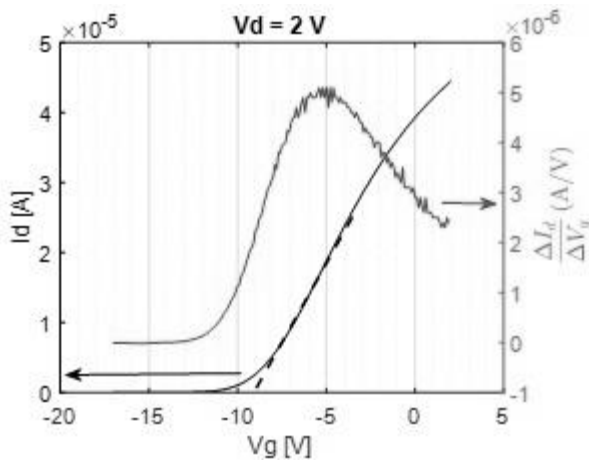


Fig. 5: Transfer Characteristics and transconductance (red curve) of fabricated IGZO TFT for $W/L = 30\mu\text{m}/2\mu\text{m}$.

The output and transfer characteristics of the fabricated IGZO TFT with gate lengths of $L=2\mu\text{m}$ and $5\mu\text{m}$ are shown in Figure 6. The drain current increased as the gate length decreased, whereas all the other parameters remained constant, as shown in Figure 6. This agrees well with the transistor equation (Eq (1)) and is fundamentally because the electric field in the channel tends to increase as the gate length decreases, thereby increasing the electron drift velocity and resulting in a higher drain current. Furthermore, considering that resistance is directly related to length and inversely related to cross-sectional area, reducing the gate length will result in a decrease in the total channel resistance R_{TOT} (as observed in Table 1), consequently allowing more drain current as the gate length is decreased.

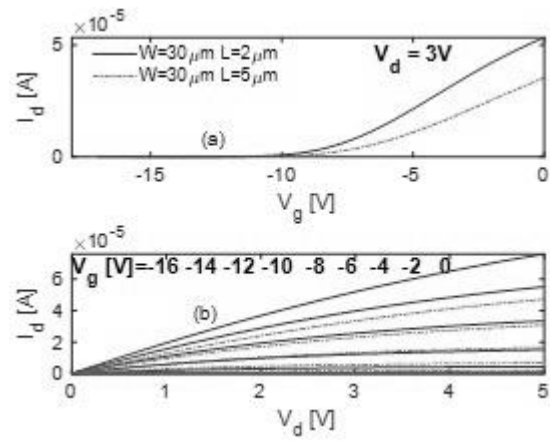


Fig. 6: (a) Transfer Characteristics and (b) Output Characteristics of Fabricated IGZO TFT for varying gate length: $L=2\mu\text{m}$ and $5\mu\text{m}$.

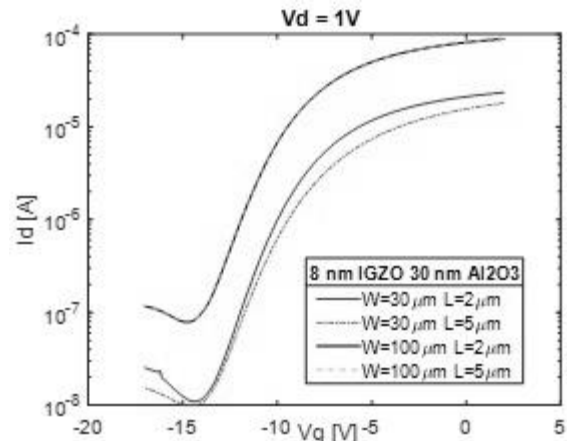


Fig. 7: Transfer Characteristics (semi logarithm scale) of Fabricated TFT with 8 nm IGZO and 30 nm Al_2O_3 and varying gate length and width.

From the transfer characteristics shown in Figure 7 and Figure 8 (with y-axis on logarithmic scale), it can clearly be observed that the device dimension with 11 nm IGZO and 20 nm Al_2O_3 shows a poor on/off current ratio compared with the 8 nm IGZO and 30 nm Al_2O_3 . The maximum ON-OFF ratio at $V_d = 1$ V was determined to be 2099 for $W/L = 30\mu\text{m} / 2\mu\text{m}$ with 8 nm IGZO and 30 nm Al_2O_3 . In addition, increasing width of the transistor tends to allow more drain current, but decreases the ON-OFF ratio. This suggests that the optimal thickness of the insulating barrier, active medium (IGZO), and device dimensions are critical for the TFT to control the drain current properly using the applied gate voltage.

A plot of the transconductance (g_m) versus gate voltage is shown in Figure 9. Because the transconductance is highly dependent on the applied electric field, the maximum value shown in Figure 9 was used to obtain the electron mobility. The maximum mobility obtained is within the range reported (Zhao, et. al., 2020), some of the parameters, such as the ON-OFF ratio and sub-threshold voltage, can be improved if the bias is increased because the measurement range is limited to $+5$ V. For the best transistor dimensions, various parameters were extracted, including threshold voltage, transconductance (g_m), sub-threshold swing, on-off ratio, mobility, interface trap density, and total channel resistance (R_{TOT}). The results for these parameters are presented in Table 1.

Table 1. Best parameters extracted for TFT device: IGZO = 8 nm, Al₂O₃ = 30 nm, W= 30 μm at Vd = 3 V

Gate Length	Threshold voltage (V)	ON-OFF ratio	Maximum g_m (AV ⁻¹)	Mobility, (μ_n) (cm ² V ⁻¹ s ⁻¹)	Sub-threshold Swing (mV/decade)	Interface trap density D_{it} (cm ⁻² eV ⁻¹)	Total channel resistance R_{TOT} (kΩ)
L = 2 μm	-9.0	4679	7.1×10^{-6}	0.63	1800	1.37×10^{14}	32
L = 5 μm	-8.3	6003	5.2×10^{-6}	1.15	2000	1.53×10^{14}	39.9

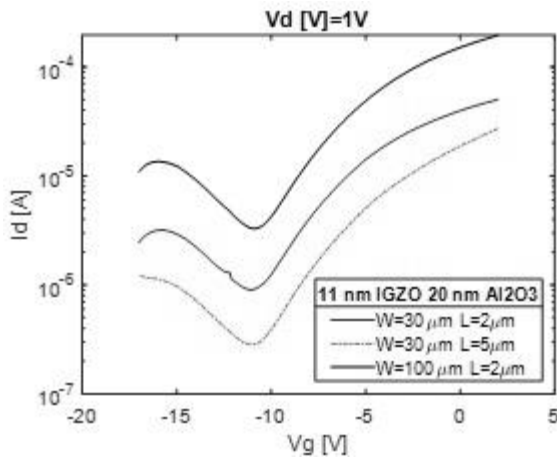


Fig. 8: Transfer Characteristics (semi logarithm scale) of Fabricated TFT with 11 nm IGZO and 20 nm Al₂O₃ and varying gate length and width.

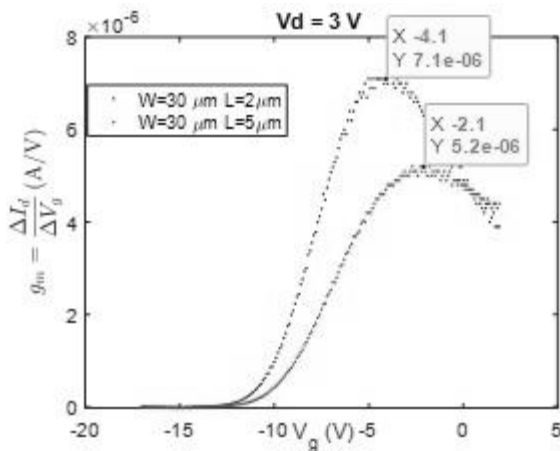


Fig. 9: Plot of gm against gate voltage for 8 nm IGZO and 30 nm Al₂O₃ and varying gate length and width.

4 CONCLUSION

We developed TCTG structure InGaZnO TFTs using a simple lithography mask process with three masks. The electrical characteristics of the fabricated TFTs was investigated and the result shows transistor parameters with a threshold voltage of -9 V, ON-OFF ratio of in the range of 10³, maximum mobility of 1.15 cm²V⁻¹ seconds⁻¹, a sub-threshold slope of in the range of 10³ milliVolts/ decade, and a maximum interface trap density of 1.53 × 10¹⁴ (cm⁻²eV⁻¹). The device parameters were also limited by the applied bias voltage because the measurement was taken up to a maximum bias of + 5 V. Also, the performance could be improved with further device geometry optimization. Reducing the processing steps will minimize the cost, particularly in the

large-scale production of TFTs for display and sensor applications.

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